In the Claims:

Claims 1-21 (Canceled).

22. (Currently amended) A method of operating a content addressable memory (CAM) array, comprising the step of:

writing ~~a xR segment of a first row in the CAM array with~~ a xR segment of a first write word into a xR segment of a first row in the CAM array while concurrently searching a xS segment of the same CAM array with a xS segment of a first search word.

23. (Currently amended) The method of Claim 22, wherein said step of writing a xR segment of a first write word ~~row in the CAM array~~ is preceded by the step of searching a xR segment of the CAM array with a xR segment of the first search word.

24. (Currently amended) The method of Claim 23, wherein said step of writing a xR segment of a first write word ~~row in the CAM array~~ is followed by the step of searching the xR segment of the CAM array with a xR segment of a second search word while concurrently writing ~~a xS segment of the first row with~~ a xS segment of the first write word into a xS segment of the first row.

25. (Currently amended) A method of operating a content addressable memory (CAM) array, comprising the step of:

reading data from a xR segment of a first row in the CAM array while concurrently searching a xS segment of the same CAM array with a xS segment of a first search word.

26. (Currently amended) The method of Claim 25, wherein said step of reading data from a xR segment of a first row in the CAM array is preceded by the step of searching a xR segment of the CAM array with a xR segment of the first search word.

27. (Currently amended) The method of Claim 26, wherein said step of reading data from a xR segment of a first row in the CAM array is followed by the step of searching the xR segment of the CAM array with a xR segment of a second search word while concurrently reading data from a xS segment of the first row.

28. (Currently amended) A method of operating a content addressable memory (CAM) array, comprising the step of:

writing ~~a xR segment of a first row in the CAM array with a~~ xR segment of a first write word into a xR segment of a first row in the CAM array while concurrently searching a xS segment of the CAM array with a xS segment of a first search word and reading data from a xT segment of a second row in the CAM array.

29. (Currently amended) A method of operating a content addressable memory (CAM) array, comprising the step of:

writing ~~a xR segment of a first row in the CAM array with a~~ xR segment of a first write word into a xR segment of a first row in the CAM array while concurrently writing a xS segment of a second write word into a xS segment of a second row in the same CAM array.

Claims 30-58 (Canceled).

59. (Original) A content addressable memory (CAM) device, comprising:

a CAM array having a first plurality of columns that define a xR segment and a second plurality of columns that define a xS segment therein; and

a interface circuit extending between the xR and xS segments of said CAM array, said interface circuit comprising:

a segment-to-segment match line control circuit having a first plurality of latches therein that are configured to store match line information derived from the xR segment of said CAM array during a xR search operation; and

a segment-to-segment word line control circuit having a second plurality of latches therein that are configured to store word line information derived from the xR segment of said CAM array during a xR write operation.

60. (Original) The CAM device of Claim 59, wherein the first plurality of latches are responsive to at least a first capture control signal.

61. (Original) The CAM device of Claim 59, wherein the first plurality of latches are responsive to at least one capture control signal; and wherein the second plurality of latches are responsive to at least another capture control signal.

62. (Original) The CAM device of Claim 59, wherein said segment-to-segment match line control circuit further comprises a plurality of NMOS pull-down transistors having gate terminals that are electrically coupled to outputs of the first plurality of latches and drain terminals that are electrically coupled to respective xS match line segments within the xS segment of said CAM array.

63. (Currently amended) The CAM device of Claim 59 **[[58]]**, wherein said segment-to-segment match line control circuit is configured to pass the stored match line information to the xS segment of said CAM array as active or inactive match line pull-down signals.

Claim 64 (Canceled).

65. (Previously presented) A content addressable memory (CAM) device, comprising:

at least one CAM array block that is configured to support writing of a xR segment of a first write word into a first row of the CAM array block while an operation is concurrently performed to search a xS segment of the same CAM array block with a xS segment of a first search word.